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LATCH-UP DETECTION AND MITIGATION IN SEMICONDUCTOR ELECTRONICS

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ABSTRACT: In semiconductors, the original signal from a noisy or distorted version is retrieved by the signal recovery process. Inthe existing studies,latch-up resistance inComplementary Metal-Oxide-Semiconductor (CMOS) devices was not focused, resulting in high power consumption. Hence,this paper proposes latch-up resistance mitigation and defect identification-based signal recovery in semiconductor electronics using a Log Bump Fuzzy Logic System (LB-FIS) and AdaptiveQuadratic Linear Log Cosh-based Deep Neural Network(AQL2C-DNN). Primarily, CMOS devices are gathered. After that, the boundaries of the p-well and n-well are detected. Then, the distance betwixt p-well and n-well is computed. Further, by using LB-FLS, latch-up resistance is detected. Afterward, the detected latch-up resistance is mitigated by inserting the guard rings. Similarly, by using AQL2C-DNN, the CMOS device defect is identified. If the device has a defect, then the alert is sent to field service engineers. If the device is normal, then layout extraction and signal path identification are done by maze routing. The best path is selected based on the Arnold Cat–CrayFish Optimization Algorithm (AC^2FOA). UsingExponential Decay Active Equalization(ED-AE), the interference is removed. Thereafter, by usingaSliding Window Averaging Phase-Locked Loop(SWA-PLL), phase compensation is performed. Subsequently, the signal is amplified and recovered at the receiver side. According to the outcomes, the proposed model obtained a low fuzzification time (674ms), thus performing better than the prevailing techniques.

KEYWORDS: *AdaptiveQuadratic Linear Log Cosh-based Deep Neural Network (AQL2C-DNN), Latch-up resistance, Log Bump Fuzzy Logic System (LB-FLS), Complementary Metal-Oxide-Semiconductor (CMOS), Arnold Cat–CrayFish Optimization Algorithm (AC^2FOA), Exponential Decay Active Equalization (ED-AE), Sliding Window Averaging Phase-Locked Loop (SWA-PLL), and Inter Symbol Interference (ISI).*

1. INTRODUCTION

Semiconductor Device (SD) fabrication has rapidly grown in recent times,which improves the power density in converters (Shan et al., 2024) (Wu et al., 2023). Power SD is the vital one for power electronic systems,which offer high-frequency operations(Nguyen & Kwak, 2020) (Zhan et al., 2023). Nevertheless, to enhance the system's resilience, SD is integrated with renewable energy sources (Athwer& Darwish, 2023). The wafer acceptance test is basically a promising factor in the semiconductor manufacturing process (Jiang et al., 2020). CMOS transistors comprise both p-type and n-type wells, which are utilized forachieving low-power dissipation (Palinje& Sinha, 2022).

In semiconductor systems, Ultra-Low-Power (ULP) image signal processors play a vital role in handling imaging tasks with minimal energy consumption (An et al., 2021). Further, to identify the abnormal operations in the SD, the Artificial Neural Network (ANN) was utilized in the existing work (Leon-Ruiz et al., 2024). Advanced Processing Control (APC) was employed in (Chen et al., 2024) to optimize the semiconductor manufacturing process. Yet, none of the prevailing methods concentrated on latch-up

resistance in CMOS devices. Hence, a latch-up resistance mitigation and defect identification-based signal recovery in semiconductor electronics using LB-FLS and AQL2C-DNN is proposed in this paper.

1.1 PROBLEM STATEMENT

- None of the traditional models focused on latch-up resistance in CMOS devices, thus causing maximum power consumption.
- Due to the inter-symbol interference issues, the existing (Guran et al., 2023) was less effective.
- The prevailing (Mesgari et al., 2024) had signal loss due to the unsynchronization in the phase response.
- Owing to the defective CMOS device, numerous conventional models had complete circuit failure.

1.2 OBJECTIVES

- To identify the latch-up resistance, the proposed LB-FLS is used. Subsequently, n-well and p-well guard rings are installed to diminish the impacts of the latch-up resistance.
- To eradicate the signal interferences, a novel ED-AE is employed.
- Here, phase compensation is carried outusing the SWA-PLL.
- The proposed AQL2C-DNN efficiently identifies the defects in the semiconductor structure.

The paper is organized as:The related models are exhibited in Section 2; the proposed mechanism is derived in Section 3; the proposed work's efficiency is validated in Section 4;the article is concluded in Section 5.

2.LITERATURE SURVEY

(Guran et al., 2023) analyzed a frequency estimation model for clock synchronization in simulators. The signal frequency and duty cycle of the Simulation Program for Integrated Circuits Emphasis (SPICE) were accurately measured by this model with minimum simulation time. However, inter-symbol interference was caused by the signal distortion, thus leading to errors.

(Mesgari et al., 2024) offered a 4Gb/s multi-dot photodiode-powered CMOS optical receiver based on a single to differential trans-impedance amplifier equalizer. The frequency roll-off of the photodiode was upgraded by this framework, thus resulting in maximum front-end bandwidth. Yet, phase response variations in the SD led to significant data loss.

(Mehta et al., 2020) developed an autoencoder-based semiconductor variation identification and inverse design. A Machine Learning (ML)-based autoencoder model was established for identifying the variations in the semiconductor structure byinvestigating the current-voltage curves. The overfitting issues were effectively mitigated by this model. Nevertheless, due to the non-linear relationship, this model had high complexity.

(Park et al., 2021) established an ML-based edge detection model for image signal processor enhancement. To improve the quality of the CMOS sensor data, this model was generalized well enough. However, this framework failed to identify the defects in the CMOS device, thus leading to signal attenuation.

(Sun et al., 2022) employed an optical phase conjugation conversion via a non-linear bidirectional semiconductor optical amplifier sub-system. This framework had error-free conjugation conversion. Nevertheless, due to the limited gain bandwidth, this framework was inadequate to handle wide-bandwidth optical systems.

3. PROPOSED FRAMEWORK

In this section, the proposed LB-FLS is introduced for detecting the latch-up resistance. Figure 1 exhibits the proposed model's architectural diagram.

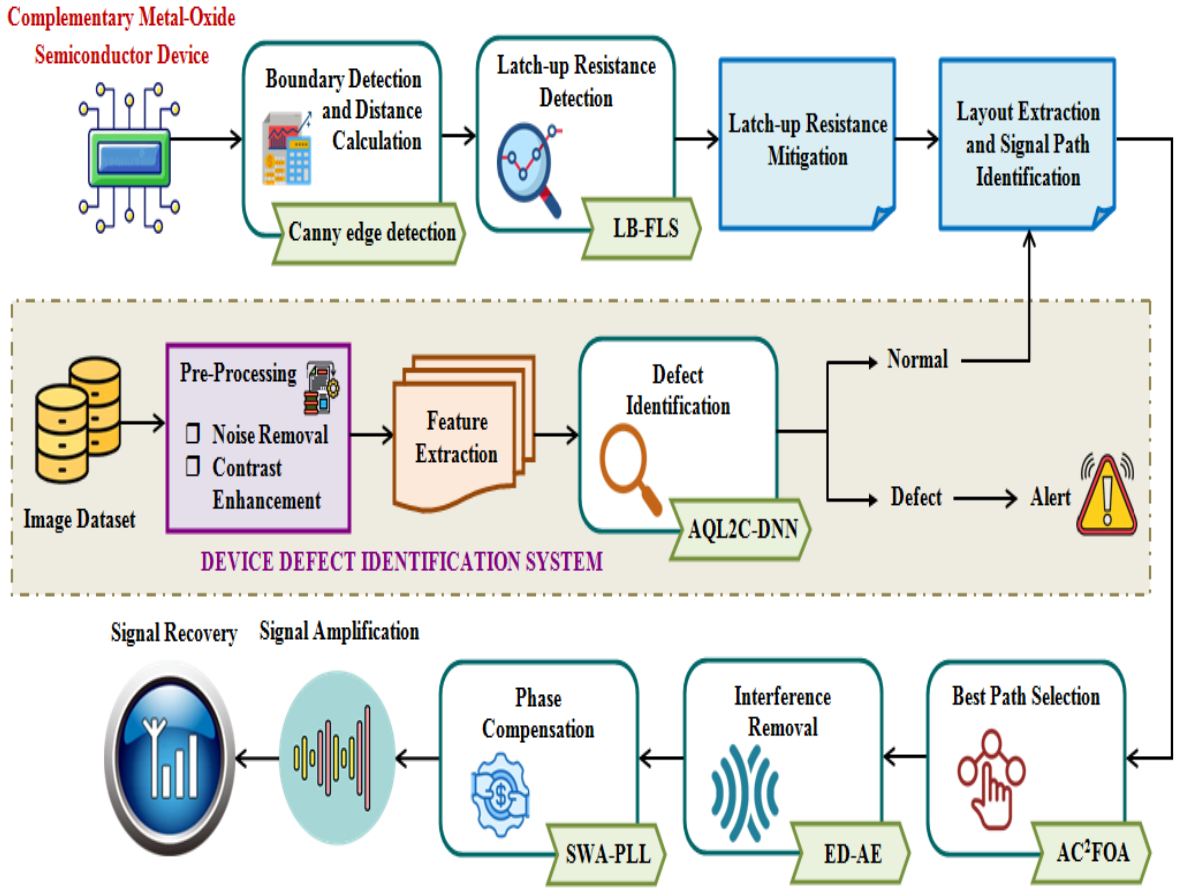


Figure 1: Architectural diagram of the proposed model

3.1 CMOS DEVICE

Firstly, for effective signal recovery, the CMOS devices are gathered.The CMOS devices $\left(\beta_u^{CMOS}\right)$ arespecified as,

$$\beta_u^{CMOS} = \left[\beta_1^{CMOS}, \beta_2^{CMOS}, \beta_3^{CMOS}, \ldots\ldots, \beta_m^{CMOS}\right] \quad (1)$$

Where, the number of $\left(\beta_u^{CMOS}\right)$ is signified as β_m^{CMOS}.

3.2 BOUNDARY DETECTION AND DISTANCE CALCULATION

Further, by using canny edge detection, the boundaries of the p-well (P_{we}) and n-well (N_{ll}) in (β_u^{CMOS}) are detected. In general, canny edge detection is beneficialtocorrectly map the shapes and orientations of p-well and n-well boundaries.

The high-frequency noises in (P_{we}) and (N_{ll}) are eliminated by utilizing the Gaussian Filter.

$$H(P_{we}, N_{ll}) = \frac{1}{2\pi s^2} \times \exp\left[-\frac{(P_{we})^2 + (N_{ll})^2}{2s^2}\right] \tag{2}$$

Here, the high-frequency noise removed p-well and n-well are notated as H, and the standard deviation is indicated as s. Then, the non-maximum suppression is estimated regarding the intensity gradients (ig) like intensity magnitude (im) and intensity direction and is shown as,

$$\zeta = Th(ig > im) \tag{3}$$

Where, the threshold is represented as Th. The boundaries are identified for the strong intensity gradients. Here, the detected boundaries are denoted as ζ.

After that, based on the Euclidean distance, the distance between (P_{we}) and (N_{ll}) is calculated as,

$$D_{PN}(P_{we}, N_{ll}) = \sqrt{\sum (P_{we} - N_{ll})^2} \tag{4}$$

Here, the estimated distance between p-well and n-well is represented as D_{PN}.

3.3 LATCH-UP RESISTANCE DETECTION

Thereafter, by employing LB-FLS, the latch-up resistance is detected based on the D_{PN}. A Fuzzy Logic System (FLS) is actually easier to design and implement. Nevertheless, generating a comprehensive set of rules in FLS is difficult and consumes more time. Thus, in FLS, the Log Bump membership function is employed.

By using If-Then rules, the fuzzy rules (F) are generated as,

$$F = \begin{cases} 8\mu m \le D_{PN} \le 10\mu m & Latch-up \\ D_{PN} \le 7\mu m & No\ Latch-up \end{cases} \tag{5}$$

Where, the micrometer is shown as μm. Latch-up resistance is present if the distance (D_{PN}) is nearer to 10 μm. Latch-up resistance is not present if the distance (D_{PN}) is far from 10 μm.

Then, to avoid difficulties in rule generation,the Log Bump membership function (χ) is estimated as,

$$\chi = \begin{cases} e^{-\frac{1}{1-\log(D_{PN}-\upsilon)^2}} & if\ |D_{PN}-\upsilon|<1 \\ 0 & otherwise \end{cases} \quad (6)$$

Here, the constant term is specified as υ.In the fuzzification interference unit (Ω), (F) are converted into crisp data (Cr).

$$\Omega = (F \to Cr) \quad (7)$$

Subsequently, the membership function is plotted based on the (Cr). Similarly, in the defuzzification interference unit (E), (Cr) are converted into (F).

$$E = (Cr \to F) \quad (8)$$

If latch-up resistance is present (L_r), then it is diminished.

Pseudocode for LB-FLS

Input: Distance between p-well and n-well (D_{PN})

Output: Detected latch-up resistance (L_r)

Begin

Initialize (D_{PN})

For (D_{PN})

Construct fuzzy rules

$$F = \begin{cases} 8\mu m \le D_{PN} \le 10\mu m & Latch-up \\ D_{PN} \le 7\mu m & No\ Latch-up \end{cases}$$

Compute Log Bump membership function

$$\chi = \begin{cases} e^{-\frac{1}{1-\log(D_{PN}-\upsilon)^2}} & if\ |D_{PN}-\upsilon|<1 \\ 0 & otherwise \end{cases}$$

Perform interference operations

Implement

$$\Omega = (F \to Cr)$$

Estimate

$$E = (Cr \to F)$$

End For

Obtain (L_r)

End

Further, layout extraction and signal path identification are done if there is no latch-up resistance (NL_{res}) .

3.4 LATCH-UP RESISTANCE MITIGATION

Afterward, L_r is mitigated by inserting the guard rings. Here, the guard rings reduce the latch-up resistance byoffering isolation for parasitic structures. $\aleph_n$ indicates the latch-up resistance mitigated CMOS device.

3.5 DEVICE DEFECT IDENTIFICATION SYSTEM

Further, the defect of the CMOS device is identified. Here, the device defect identification system is trained as shown below,

3.5.1 DATASET

Initially, the "Device defect identification" image dataset is gathered and is signified as δ_l.

3.5.2 PRE-PEOCESSING

After that, the δ_l is pre-processed. Primarily, by using a median filter, the unwanted noises in δ_l are removed. The noise-removed image $\left(\tilde{\lambda}(v,w)\right)$ is expressed as,

$$\tilde{\lambda}(v,w) = \underset{(a,b)\in\delta_l}{median}\{gu(a,b)\} \tag{9}$$

Where, the Gaussian function is specified as gu, and the pixel coordinates of the input image are displayed as (a,b). Then, the contrast of $\left(\tilde{\lambda}(v,w)\right)$ is enhanced.Lastly, $\wp_\kappa$ represents the obtained pre-processed images.

3.5.3 FEATURE EXTRACTION

The features like resistance, parasitic capacitance, junction leakage, defect density, and short circuit power dissipation are extracted from $\wp_\kappa$. The extracted features are specified as Fe_j.

3.5.4 DEFECT IDENTIFICATION

By employing AQL2C-DNN,device defect identification is done based on Fe_j. Hierarchical features from raw image data could be automatically learned by Deep Neural Networks (DNNs). Nevertheless, DNNs can overfit the training data, thus causing poor generalization. Hence, in DNN, the Adaptive Quadratic Linear unit (AQL) activation function and Log Cosh regularization are employed. In Figure 2, the AQL2C-DNN classifier is depicted.

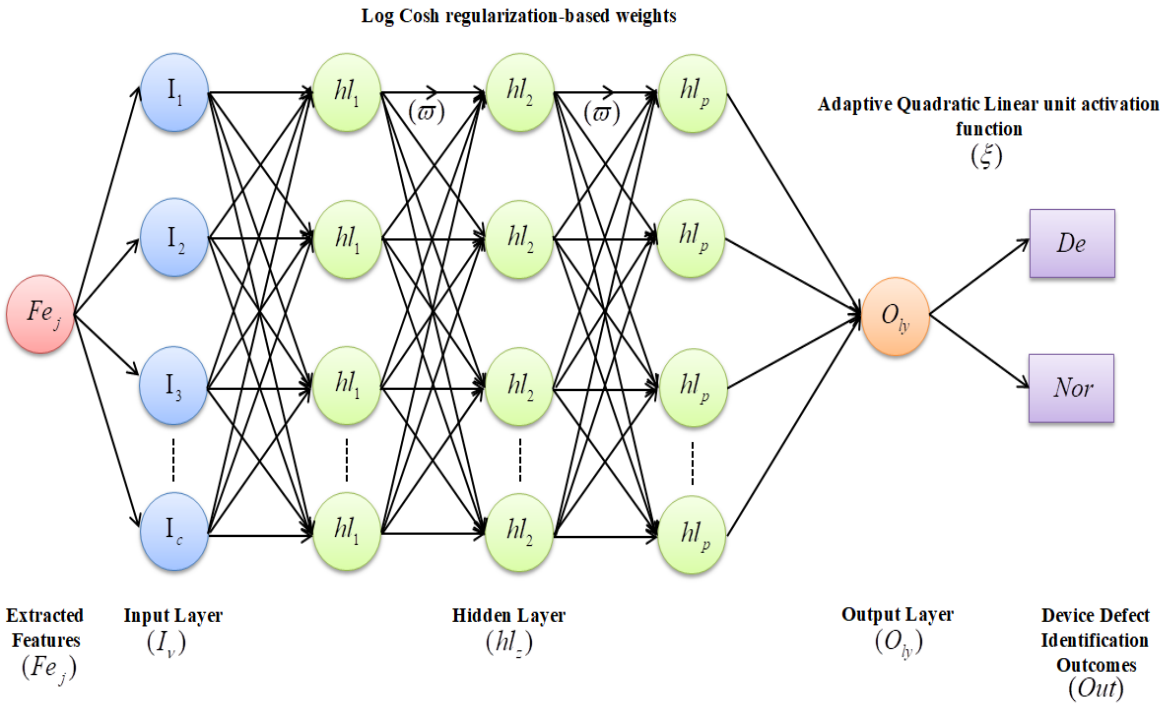


Figure 2:AQL2C-DNN classifier

Input layer: The input layer holds the input Fe_j and further passes it through the hidden layer.

$$I_v\left(Fe_j\right)\rightarrow\left[I_1+I_2+I_3+\ldots\ldots+I_c\right] \tag{10}$$

Where, the number of the input layer $\left(I_v\right)$ is indicated as I_c.

Hidden layer: Then, the p number of hidden layers $\left(hl_z\right)$ grasps the I_v and is given for further process.

$$hl_z=\xi\left(\varpi^{hl}\cdot I_v+B^{hl}\right) \tag{11}$$

Here, the weights and biases in the hidden layer are specified as ϖ^{hl} and B^{hl}, respectively, and the AQL activation function is represented as ξ.

$$\xi=\begin{cases} I_v & if\ I_v\geq\dfrac{1-Z}{Y} \\ Y\left(I_v\right)^2+ZI_v & if\ -\dfrac{Z}{Y}\leq I_v<\dfrac{1-Z}{Y} \\ 0 & if\ I_v<-\dfrac{Z}{Y} \end{cases} \tag{12}$$

Where, the constant terms are notated as Z and Y. By using Log Cosh regularization, the weights (ϖ) are initialized and are given as,

$$\varpi=Ls+rh\sum\log\left(\cosh\left(I_v\right)\right) \tag{13}$$

Here, the loss function is signified as Ls, the regularization hyperparameter is displayed as rh, and the hyperbolic cosine function is depicted as cosh.

Output layer: The output layer (O_{ly}) excellently detects whether the defect is present in the CMOS devices or not.

$$O_{ly} = \xi\left(\varpi^{O} \cdot hl_{z} + B^{O}\right) \tag{14}$$

$$Out = \langle De, Nor \rangle \tag{15}$$

Where, the device defect identification outcomes are implied as Out, De indicates that the device has a defect, and Nor specifies that the device is normal.

Pseudocode for AQL2C-DNN

Input: Extracted Features (Fe_{j})

Output: Device defect identification outcomes (Out)

Begin:

Initialize (Fe_{j}) and (B)

Set $[iter == 1]$

While $(iter \le iter^{\max})$

Perform (I_{v})

For 1 to p hidden layers

Implement $hl_{z} = \xi\left(\varpi^{hl} \cdot I_{v} + B^{hl}\right)$

Find $\xi = \begin{cases} I_{v} & if\ I_{v} \ge \dfrac{1-Z}{Y} \\ Y(I_{v})^{2} + ZI_{v} & if\ -\dfrac{Z}{Y} \le I_{v} < \dfrac{1-Z}{Y} \\ 0 & if\ I_{v} < -\dfrac{Z}{Y} \end{cases}$

Initialize $\varpi = Ls + rh\sum \log\left(\cosh\left(I_{v}\right)\right)$

End For

Estimate (O_{ly})

End While

Obtain $Out = \langle De, Nor \rangle$

End

The SD image (Se_{im}) is taken in real-timeduring testing. Also,based on the aforementioned processes, the defect is identified. If De, then the alert is sent to field service engineers. If Nor, then layout extraction is carried out.

3.6 LAYOUT EXTRACTION AND SIGNAL PATH IDENTIFICATION

From $\aleph_n$, the layout is extracted if the device has latch-up resistance. From the normal CMOS device (α_{ml}), the layout is extracted if (NL_{res}). K_ς represents the extracted layouts.

Then, from K_ς, the signal path is identified by using Maze routing. Primarily, the source cell and wavefront queue are initialized. After that, by incrementing distances for reachable neighbors, the wavefront is expanded. Then, the shortest path is constructed. Lastly, the identified signal path is represented as N_μ .

3.7 BEST PATH SELECTION

For effective transmission, the optimal path is selected from N_μ by usingAC^{2}FOA. The likelihood of getting trapped in local optima is effectively reduced by the Cray Fish Optimization Algorithm (CFOA). Yet, ithasa premature convergence issue. Hence, Arnold cat map is employed.

Primarily, the population of crayfish groups is initialized. The initialized population is regarded as the identified signal path.

$$V_{d,q} \xrightarrow{N_\mu} low + R \times (up - low) \tag{16}$$

Where, the initialized population of crayfish is represented as $V_{d,q}$, the random number is indicated as R, and the lower and upper bounds are represented as low and up, respectively. Thereafter, the fitness function is computed by considering the minimum distance.

When the temperature is more than 30 degrees, a cool place is chosen by the crayfish to avoid heat.Crayfish enter the cave during the summer vacation phase for avoiding the heat $(V_{d,q}^{new1})$, and their competitive behaviors $(V_{d,q}^{new2})$arearticulated as,

$$V_{d,q}^{new1} = V_{d,q} + \left(2 - \left(\frac{it}{ite+1}\right)\right) \times A \times (V_{cv} - V_{d,q}) \tag{17}$$

$$A = \begin{pmatrix} 1 & 1 \\ 1 & 2 \end{pmatrix} \begin{pmatrix} V_{d,q} \\ V_{cv} \end{pmatrix} \quad \text{mod } 1 \tag{18}$$

$$V_{d,q}^{new2} = V_{d,q} - V_{f,q} + V_{cv} \tag{19}$$

Here, the current iteration is notated as it, the maximum iteration is specified as $ite+1$, the summering behavior is denoted as V_{cv}, and the Arnold cat map is represented as A.

If the temperature is less than or equal to 30 degrees Celsius, then it is suitable for crayfish foraging.

$$V_{d,q}^{new3} = V_{d,q} + \exp\left(-\frac{1}{S}\right) \times V_{Mbest} \times pb \times (\cos(2 \times \pi \times R) - (\sin 2 \times \pi \times R)) \tag{20}$$

$$V_{d,q}^{new4} = (V_{d,q} - V_{Mbest}) \times pb + pb \times R \times V_{d,q} \tag{21}$$

Where, the foraging behavior is notated as $V_{d,q}^{new3}$, the eating behavior of crayfish is represented as $V_{d,q}^{new4}$, the food picking of crayfish is specified as S, the best position is denoted as V_{Mbest}, and the crayfish feeding is shown as pb. ϑ_h specifies the selected best path.

3.8 INTERFERENCE REMOVAL

Further, to avoid errors,interference in the ϑ_h are removed by utilizing ED-AE. The quality of signals could be significantly enhanced by Active Equalization (AE). However,due to processing time, AE introduces latency. Thus, Exponential decay is employed.

The signal $(g(t))$ is signified as,

$$g(t) \xrightarrow{\vartheta_h} di(t) + \text{int}(t) + ns(t) \tag{22}$$

Here, the desired signal is depicted as $di(t)$, the interference is given as $\text{int}(t)$, and the noise is specified as $ns(t)$. Thereafter, the signal-to-interference-plus noise ratio is maximized by the equalization filter. Here, to improve the latency, the Exponential decay $(\xi\chi)$is applied.

$$U(fq) = 1 - \frac{(fq)^2}{(fq)^2 + 2\varepsilon(fq)(fq)_0 + (fq)_0^2} \times \xi\chi \tag{23}$$

$$\xi\chi = \xi\chi_0 e^{-it} \tag{24}$$

Where, the frequency is represented as fq, the interference frequency is implied as $(fq)_0$,the damping factor is depicted as ε, the decay constant is specified as i, and $\xi\chi_0$ specifies the initial quantity. Thus, the interference-removed signal is indicated as J_φ.

3.9 PHASE COMPENSATION

Next, for J_φ, the phase compensation is doneby using SWA-PLL. In phase alignment, Phase-Locked Loops (PLLs) achieve high accuracy. PLL may fail to lock if the frequency of the input signal deviates too much. Hence, in PLL, sliding window averaging is utilized.

Initially, the phase detector output $(X_{pha}(\tau))$is assessed. Here, to improve the phase compensation, the sliding window averaging (ςw) is added.

$$X_{pha}(\tau) \xrightarrow{J_\varphi} G_{in} \cdot \phi(\tau) + \varsigma w \tag{25}$$

$$\varsigma w = \frac{1}{W} \sum_{\varphi} J_\varphi \tag{26}$$

Here, the gain of the phase detector is exemplified as G_{in}, the phase difference is depicted as $\phi(\tau)$, and the window size is notated as W. Further, the control signal is smoothened by the loop filter. Then, the closed-loop transfer function $(T^*(x))$ of the PLL is given as,

$$T^*(x) = \frac{G_{in}G_{VCO}\tilde{\chi}(x)}{x + G_{in}G_{VCO}\tilde{\chi}(x)} \quad (27)$$

Where, the gain of the Voltage Controlled Oscillator (VCO) is displayed as G_{VCO} ,the loop filter transfer function is signified as $\tilde{\chi}(x)$, and the variable is denoted as x. The phase compensated signal is specified as Ψ_{pc}.

3.10 SIGNAL AMPLIFICATION

Further, Ψ_{pc} is amplified. At last, the amplified signal (Am) is recovered at the receiver side. Therefore, an efficientsignal recovery is carried out in semiconductor electronics.

4. RESULTS AND DISCUSSION

Here, the proposed work'sprominence is demonstrated through the performance analysis. The experimentation is carried out on the MATLAB platform.

4.1 DATASET DESCRIPTION

By using the semiconductor wafer map defect identification dataset, the proposed work is implemented. Here, from the whole data, 80% of the data is allocated for training andthe remaining 20% of the data is allocated for testing.

4.2 PERFORMANCE ASSESSMENNT

To showcase the model's trustworthiness, a performance analysis is done.

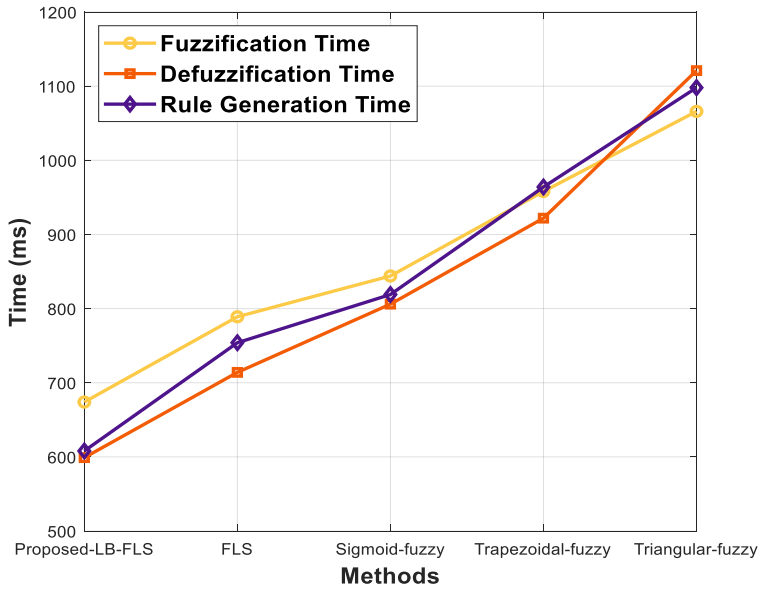
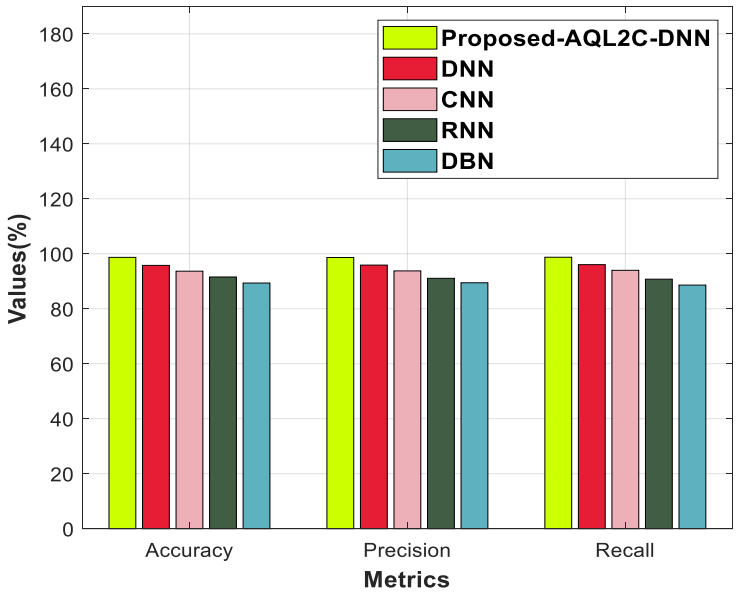
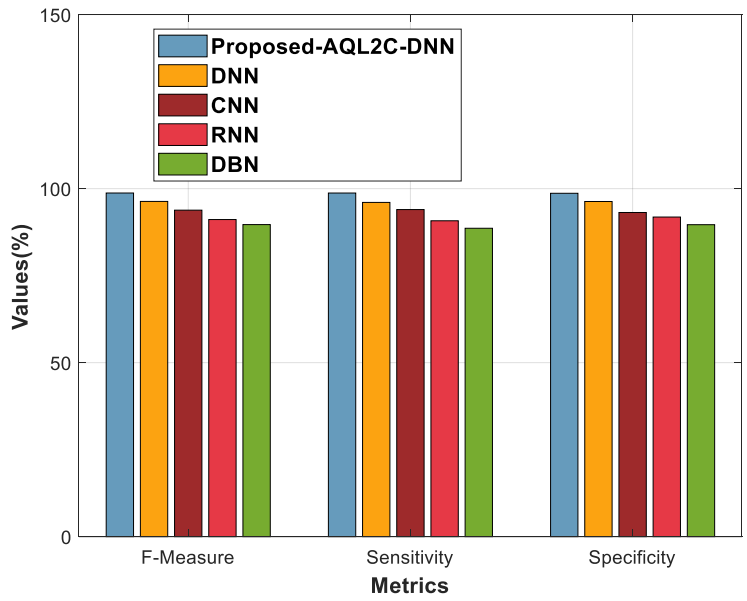


Figure 3: Performance validation of the proposed LB-FLS

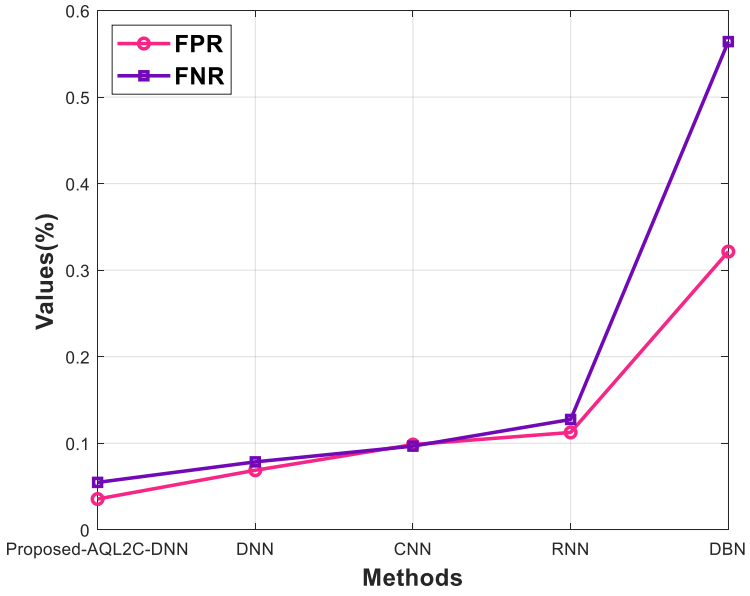
The performance of the proposed LB-FLS and conventional techniques like FLS, sigmoid-fuzzy, trapezoidal-fuzzy, and triangular-fuzzy is analyzed in Figure 3. The proposed LB-FLS had a Fuzzification Time (FT) of 674ms, Defuzzification Time (DT) of 599ms, and Rule Generation Time (RGT) of 608ms. Nevertheless, the prevailing triangular-fuzzy had FT, DT, and RGT of 1066ms, 1121ms, and 1098ms, respectively. Hence, due to the presence of Log Bump (LB) membership,the proposed method had low time complexity in latch-up resistance detection.



(a)



(b)



(c)

Figure 4 (a) (b) and (c): Performance validation for defect identification

In Figure 4, the performance of the proposed AQL2C-DNN is assessed by comparing it with existing classifiers like DNN, Convolutional Neural Network (CNN), Recurrent Neural Network (RNN), and Data Belief Network (DBN). The proposed AQL2C-DNN obtained accuracy, precision, recall, f-measure, sensitivity, specificity, False Positive Rate (FPR), and False Negative Rate (FNR) of 98.96%, 98.66%, 98.74%, 98.74%, 98.74%, 98.66%, 0.035 and 0.054, respectively. Yet, owing to poor generalization, the traditional classifiers had limited performance. Hence, the proposed method had impressive outcomes owing to the use of AQuLU activation.

Table 1: Training time

Method	Training Time (ms)
Proposed AQL2C-DNN	5841
DNN	6317
CNN	7884
RNN	8754
DBN	9869

Table 1 compares the training time of the proposed AQL2C-DNN and existing algorithms. The proposed AQL2C-DNN had a training time of 5841ms, whereas the existing methods had amean training time of 8206ms. Thus, the proposed method had higher superiority.

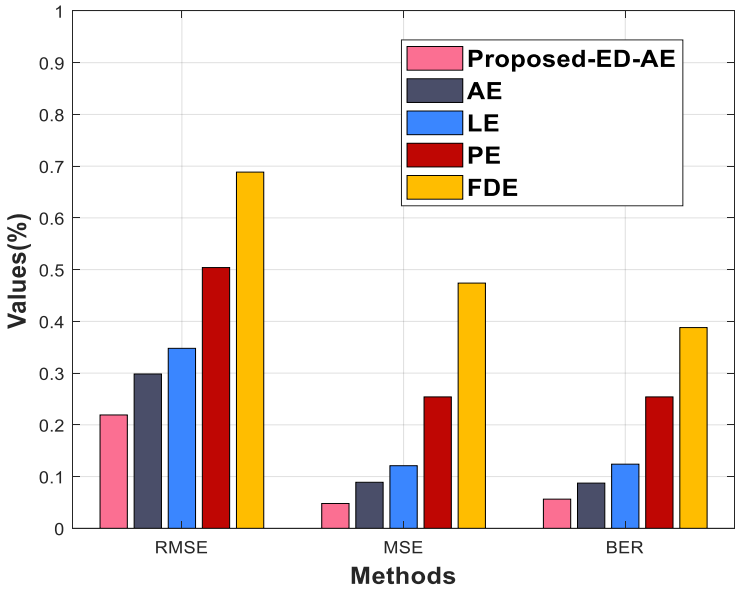


Figure 5: Performance assessment for interference removal

Figure 5 presents the error rate analysis of the proposed ED-AE and existing algorithms like AE, Linear Equalization (LE), Passive Equalization (PE), and Frequency Domain Equalization (FDE). The proposed ED-AE obtained a Root Mean Squared Error (RMSE) of 0.2191, Mean Squared Error (MSE) of 0.048, and Bit Error Rate (BER) of 0.0564. Yet, the existing AE attained an RMSE of 0.2983, MSE of 0.089, and BER of 0.0874. Lastly, when compared to the prevailing studies, the proposed framework had fewer errors.

Table 2: Path selection time analysis

Method	Path Selection Time(ms)
Proposed AC^{2}FOA	5614
CFOA	6251
COA	7567
JOA	8548
STO	9969

In Table 2, the path selection time assessment of the proposed AC^{2}FOA and conventional algorithms,such as CFOA, Coati Optimization Algorithm (COA), Jellyfish Optimization Algorithm (JOA), and Siberian Tiger Optimization (STO) is exhibited. To select the optimal path, the proposed AC^{2}FOA took 5614ms, whereas the traditional STO had 9969ms path selection time. Thus, the proposed methodology'sdominance was proven.

4.3 COMPARATIVE ANALYSIS

Likewise, to reveal the consistency of the proposed work, comparative validation is done.

Table 3: Comparative assessment

Author's name	Method	Accuracy (%)	Precision (%)
Proposed work	AQL2C-DNN	98.96	98.66
(Zheng et al., 2021)	Deep-CNN	93.75	93.81
(Patel et al., 2024)	Federatedlearning and explainable artificial intelligence	98.78	-
(Saqlain et al., 2020)	Deep-CNN	96.2	96.24
(Haddad et al., 2020)	DNN	97.88	-
(Chang et al., 2022)	CNN	96.97	-

Table 3 depicts the comparative analysis of the proposed work and related models. The proposed AQL2C-DNN obtained an accuracy of 98.96% and a precision of 98.66%. However, the existing Deep-CNN (Zheng et al., 2021) achieved accuracy and precision of 93.75% and 93.81%, respectively. Owing to the overfitting issues, the existing works were ineffective. Hence, in defect identification, the proposed work had higher supremacy.

5. CONCLUSION

In this paper, a latch-up resistance-aware defect detection-based signal recovery in semiconductor electronics using LB-FLS and AQL2C-DNN was proposed.The latch-up resistance was effectively estimated by the proposed LB-FLS, thus mitigating the power loss. Here, to increase the resilience of the model, latch-up mitigation and phase compensation were done. Similarly, to identify the defect in the semiconductor electronics, the proposed AQL2C-DNN was employed, which improved the model's stability and communication. Hence, as per the evaluation outcomes, the proposed framework had an accuracy of 98.967%, RGT of 608ms, and RMSE of 0.2191, exhibiting high efficiency and low complexity.

Future scope: This work will focus on designing secure chips in the future to resist software attacks, enhancing the performance of the semiconductor technology.

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Dataset:

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